WHAT IS CLAIMED IS:

1. A method for configuring an analog-to-digital converter, comprising:

receiving a control signal and an input analog signal at an analog-to-digital converter, the control signal having a state selected from a group consisting of a first state and a second state, the first state associated with a first configuration, the second state associated with a second configuration, the input analog signal comprising information;

performing the following if the control signal has the first state:

configuring the analog-to-digital-converter in the first configuration in response to the control signal; and

generating a digital signal comprising a first digital signal according to a pipeline conversion;

performing the following if the control signal has the second state:

configuring the analog-to-digital converter in the second configuration in response to the control signal; and

generating the digital signal comprising a second digital signal according to a multi-stage sigma delta modulation conversion; and

processing the digital signal to yield a digital output, the digital output comprising the information.

2. The method of Claim 1, wherein the first configuration comprises a pipeline analog-to-digital converter configuration.

3. The method of Claim 1, wherein the second configuration comprises a multi-stage noise shaping analog-to-digital converter configuration.

4. The method of Claim 1, wherein generating the first digital signal comprises:

repeating the following for each stage of a plurality of stages:

convert a residual analog signal of a previous stage to a coarse digital signal;

convert the coarse digital signal to a coarse analog signal; and

sum the analog signal and the coarse digital signal to yield a residual analog signal of a current stage; and

generating a first digital signal according to the coarse digital signals of the plurality of stages.

5. The method of Claim 1, wherein generating the second digital signal comprises:

repeating the following for each stage of a plurality of stages:

applying a sigma-delta modulation to a previous analog signal to yield a current coarse digital signal;

converting the current coarse digital signal to a current coarse analog signal;

generating a current analog signal from the current coarse analog signal; and

generating the second digital signal according to the coarse digital signals of the plurality of stages.

6. The method of Claim 1, wherein processing the digital signal to yield the digital output further comprises:

decoding the digital signal by performing error correction of the digital signal; and

generating a binary code corresponding to the decoded digital signal, the binary code comprising the information.

7. The method of Claim 1, wherein processing the digital signal to generate a digital output further comprises:

decimating the digital signal to yield an averaged digital signal, the averaged digital signal having a higher resolution than the digital signal; and

filtering the averaged digital signal to yield the digital output.

8. The method of Claim 1, wherein the first state associated with the first configuration comprises a low state of the control signal.

9. The method of Claim 1, wherein the second state associated with the second configuration comprises a high stage of the control signal.

10. An analog-to-digital converter, comprising:

an input node operable to receive a control signal and an input analog signal, the control signal having a state selected from a group consisting of a first state and a second state, the first state associated with a first configuration, the second state associated with a second configuration, the input analog signal comprising information;

a multi-stage circuit coupled to the input node and operable to:

perform the following if the control signal has the first state:

configure the analog-to-digital-converter in the first configuration in response to the control signal; and

generate a digital signal comprising a first digital signal according to a pipeline conversion;

perform the following if the control signal has the second state:

configure the analog-to-digital converter in the second configuration in response to the control signal; and

generate the digital signal comprising a second digital signal according to a multi-stage sigma delta modulation conversion; and

a digital logic block coupled to the multi-stage circuit and operable to process the digital signal to yield a digital output, the digital output comprising the information.

11. The analog-to-digital converter of Claim 10, wherein the first configuration comprises a pipeline analog-to-digital converter configuration.

12. The analog-to-digital converter of Claim 10, wherein the second configuration comprises a multi-stage noise shaping analog-to-digital converter configuration.

13. The analog-to-digital converter of Claim 10, wherein the multi-stage circuit is further operable to:

repeat the following for each stage of a plurality of stages:

convert a residual analog signal of a previous stage to a coarse digital signal;

convert the coarse digital signal to a coarse analog signal; and

sum the analog signal and the coarse digital signal to yield a residual analog signal of a current stage; and

generate a first digital signal according to the coarse digital signals of the plurality of stages.

14. The method of Claim 1, wherein the multi-stage circuit is further operable to:

repeat the following for each stage of a plurality of stages:

apply a sigma-delta modulation to a previous analog signal to yield a current coarse digital signal;

convert the current coarse digital signal to a current coarse analog signal; and

generate a current analog signal from the current coarse analog signal; and

generate the second digital signal according to the coarse digital signals of the plurality of stages.

15. The analog-to-digital converter of Claim 10, the digital logic block further operable to:

decode the digital signal by performing error correction of the digital signal; and

generate a binary code corresponding to the decoded digital signal, the binary code comprising the information.

16. The analog-to-digital converter of Claim 10, the digital logic block further operable to:

decimate the digital signal to yield an averaged digital signal, the averaged digital signal having a higher resolution than the digital signal; and

filter the averaged digital signal to yield the digital output.

17. The analog-to-digital converter of Claim 10, wherein the first state associated with the first configuration comprises a low state of the control signal.

18. The analog-to-digital converter of Claim 10, wherein the second state associated with the second configuration comprises a high stage of the control signal.

19. An analog-to-digital converter, comprising:

means for receiving a control signal and an input analog signal at an analog-to-digital converter, the control signal having a state selected from a group consisting of a first state and a second state, the first state associated with a first configuration, the second state associated with a second configuration, the input analog signal comprising information;

means for performing the following if the control signal has the first state:

configuring the analog-to-digital-converter in the first configuration in response to the control signal; and

generating a digital signal comprising a first digital signal according to a pipeline conversion;

performing the following if the control signal has the second state:

configuring the analog-to-digital converter in the second configuration in response to the control signal; and

generating the digital signal comprising a second digital signal according to a multi-stage sigma delta modulation conversion; and

means for processing the digital signal to yield a digital output, the digital output comprising the information.

20. An analog-to-digital converter, comprising:

an input node operable to receive a control signal and an input analog signal, the control signal having a state selected from a group consisting of a first state and a second state, the first state associated with a first configuration and comprising a low state of the control signal, the second state associated with a second configuration and comprising a high state of the control signal, the input analog signal comprising information;

a multi-stage circuit coupled to the input node and operable to:

perform the following if the control signal has the first state:

configure the analog-to-digital-converter in the first configuration in response to the control signal, the first configuration comprising a pipeline analog-to-digital converter configuration; and

generate a digital signal comprising a first digital signal according to a pipeline conversion by:

repeating the following for each stage of a plurality of stages:

converting a residual analog signal of a previous stage to a coarse digital signal;

converting the coarse digital signal to a coarse analog signal; and

summing the analog signal and the coarse digital signal to yield a residual analog signal of a current stage; and

generating the first digital signal according to the coarse digital signals of the plurality of stages;

perform the following if the control signal has the second state:

configure the analog-to-digital converter in the second configuration in response to the control signal, the second configuration comprising a multi-stage noise shaping analog-to-digital converter configuration; and

generate the digital signal comprising a second digital signal according to a multi-stage sigma delta modulation conversion by:

repeating the following for each stage of a plurality of stages:

applying a sigma-delta modulation to a previous analog signal to yield a current coarse digital signal;

converting the current coarse digital signal to a current coarse analog signal;

generating a current analog signal from the current coarse analog signal; and

generating the second digital signal according to the coarse digital signals of the plurality of stages; and

a digital logic block coupled to the multi-stage circuit and operable to process the digital signal to yield a digital output by:

performing the following if the control signal has the first state:

decoding the digital signal by performing error correction of the digital signal; and

generating a binary code corresponding to the decoded digital signal, the binary code comprising the information; and

performing the following if the control signal has the second state:

decimating the digital signal to yield an averaged digital signal, the averaged digital signal having a higher resolution than the digital signal; and

filtering the averaged digital signal to yield the digital output, the digital output comprising the information.